Abstract:

The present paper treats the Carbon Nanotube Field Effect Transistors (CNFETs) in terms of new development as a possible future basic element for beyond CMOS technology used in ultra high scale integration ULSI. The CNFET is studied both in physical as well as technological point of views aiming a further understanding of the limitations to high integration density. The different types of carbon nanotubes (SWNT) and (MWNT) used for electronic and sensing devices are discussed and the limitations for a higher integration density are evidenced. The CNFET switching characteristics and the IV characteristics are discussed to evidence the power dissipation and the switching frequency.

Keywords: Carbon Nanotubes, CNFET, Integrated Circuits, I-V Characteristics, NanoMOSFET

1. Introduction

The demand for higher computing power, smaller dimensions, and lower power consumption of integrated circuits leads to a pressing need to downscale semiconductor components [1]. However, shrinking device geometry of conventional MOSFETs leads to complex problems, such as short-channel effects, gate-leakage current, and high power dissipation. Therefore, novel structure and materials such as NanoMOSFETs and MGMOSFETs, CNFETs, [2,3] and Molecular Transistors, are expected to be introduced to meet the requirements for scaling. Efforts are concentrated on the CNFETs issue.

Since the discovery of carbon nanotubes (CNTs) by Ijima in the 1990s [4,5], increasing progress has been achieved in both understanding the fundamental properties and exploring possible engineering applications like device based CNTs. The possible application for nanoelectronic devices has been extensively explored since the demonstration of the first CNFETs. Figure 1 shows the different perspectives for non conventional nanoelectronics.
CNTs are attractive for nano-electronic applications due to their excellent electrical properties. The phase space for scattering is severely reduced due to the one-dimensional nature of the density of states. The low scattering probability is responsible for high on-current in semiconducting CNFETs. Due to the chemical stability and perfection of the CNT structure carrier mobility is not affected by processing and roughness scattering as it is in the conventional semi-conductor channel. The fact that there are no dangling bond states at the surface of CNTs allows for a wide choice of gate insulators. This improves gate control while meeting gate leakage constrains. The purely one-dimensional transport properties of the SWCNTs should lead to a suppression of short-channel effects in transistor devices [6]. Furthermore, the conduction and valence bands are symmetric, which is advantageous for complementary applications, and finally, the combined impact of transport and electrostatic benefits together with the fact that semiconducting CNTs are unlike silicon, direct-gap materials, suggests applications in opto-electronics as well.

2. The Carbon Nanotube Field Effect Transistor Principles

The one-dimensional nature of CNTs severely reduces the phase space for scattering, allowing CNTs to realize maximum possible bulk mobility of this material. The low scattering probability and high mobility are responsible for high on-current of CNT transistors. Furthermore, the chemical stability and perfection of the CNT structure suggests that the carrier mobility at high gate fields may not be affected by processing and roughness scattering as in the conventional semiconductor channel. Similarly, low scattering together with the strong chemical bonding and high thermal conductivity allows metallic CNTs to withstand extremely high current densities (up to $10^9$ A/cm$^2$).

Electrostatics is improved in these devices as well. The fact that there are no dangling bond states at the surface of CNTs allows for a much wider choice of gate insulators other than conventional SiO$_2$. This improved gate control without any additional gate leakage becomes very important in scaled devices with effective SiO$_2$ thickness below 1 nm. Also, the strong one-dimensional electron confinement and full depletion in the nanometer-scale diameter of the SW-CNTs (typically 1-2 nm) should lead to a suppression of short-channel effects in transistors [7]. Figure 2 shows a Graphene CNFET and Fig.3 shows that of Carbon CNFET. The CNFET and MOSFET show the same characteristics. The equivalency of CNFET and Nano MOSFET can lead to MOSFET substitution in VLSI circuits and one can deals with CNFET VLSI Circuit.

In a recent work [8] we have modeled the drain current and found it to be the same as that of the MOSFET in the critical saturation region. Finally, since CNTs can be both metallic and semiconducting, All-CNT electronics can be envisioned. In this case, metallic CNTs could act as high current carrying local interconnects while semiconducting CNTs would form the active devices.
The most important appeal of this approach is an ability to fabricate one of the critical device dimensions (the CNT diameter) reproducibly using synthetic chemistry. In a recent work on, we report our own approach of a similar study, aiming to achieve the unprecedented peapod-to-DWCNT transformation at room temperature and in open air. The results are compared with those of the literature based on both microprobe Raman spectroscopy (specifically through the 2D band) and high-resolution transmission electron microscopy (HRTEM) investigations [9].

3. CNFETs and the Integration Problem

The promising characteristics of individual CNT-FETs have lead to initial attempts at integration of several CNT-FETs into useful circuits that can perform a logic operation, or function as memories or sensors. In the following, we limit our discussion to advances in logic circuitry. The CNT logic gates have been, in most cases, based on a complementary technology analogous to silicon CMOS, which is important as it may ease integration of CNTs onto this well established technology. A typical inverter is shown in Fig.4.

The first complementary (CMOS-like) logic gates were reported by DERYCKE. In that work, two different techniques were used to produce n-type devices. An inverter gate was created by combining two CNT-FETs: a p-type device in the ambient and a vacuum annealed n-type device. A more compact and integrated approach uses potassium doping to convert one of two CNT-FETs built on the same CNT to n-type. The masking of the other transistor which remained p-type was accomplished by photo-resist. The circuit had a voltage gain of about two, suggesting that integration, without signal degradation, of many devices along a single CNT can be accomplished.

After the success of the CN Inverter, other integrated circuits came to substitute that of conventional technology. Various workers used different approaches to build p and n type CNFETs and wired the inverters to build complex ICs. Figure 5 show a full adder built using CNFETs.

The two main technology constraints that limit the viability of CNFET technology are the misaligning of CNTs and the presence of metallic CNTs among the semiconducting CNTs, while the CNTs are grown or transferred over a substrate. Metallic CNTs are highly undesirable as they short-circuit the drain and the source of the CNFET. Electrical burning and Chemical etching of the metallic CNTs are the major techniques addressed so far to remove or break them.

Zhang et al [10] derive practical processing guidelines for metallic CNT growth and removal, showing that major technology level advancement is necessary for VLSI scale CNFET circuit to be possible. Since the metallic CNT constraint would mainly be handled during the
manufacturing stage, we assume that no metallic CNT remains as starting scenario for the application of our work during the rest of the paper. On the other hand, we take up the challenge of addressing the issue of misaligned CNTs.

There are a few ways at the physical level to achieve good alignment of CNTs arrays, and a small percentage of CNTs get yet misaligned and the problem is only partly solved. In spite of superior device characteristics, CNFET circuits are difficult to realize at large scale because of some serious manufacturing challenges like variations in doping and diameter of CNTs, metallic CNTs and misaligned CNTs. Though the diameter and doping variations in CNTs cause drain current variations, the major challenge is towards handling metallic and misaligned CNTs as they affect the functionality of the gate.

Since misaligned CNTs cannot be avoided by the known CNFET manufacturing technology, many efforts are being developed to overcome this drawback. One can distinguish the new layout technique that is functionally immune to the CNT misaligning which is referred as “misaligned-CNT-immune layouts”. This will allow the production of standard VLSI cells as well as design tools that allow to go from Layouts to physical cells and then to transistors.

4. Perspectives in Nanoelectronics

CNFETs are promising in the future developments on Nanoelectronics. Large scale integrated circuits are foreseen. FPGA based on CNFETs are introduced [11]. SRAMs using nanotubes are yet produced and Optoelectronics applications such as Light emitting nanotubes are reported and produced by IBM Company. Considerable applications are yet investigated in the fields of sensing and energy conversions. Figure 6 shows a schematic diagram of a light detector and solar cell. The SWCNT light source is a three-terminal device that involves no doping and also allows control of the emission intensity and the position of the emitting spot along the length of the CNT. The diameter of the CNT defines the wavelength of the emitted light, typically in the infrared range.

The reverse process of photocurrent generation with a significant yield by photoexcitation of a CNTFET device has also been demonstrated. This single CNT device can function as an electrical switch, a light emitter, or a light detector, depending on the biasing. The carbon nanoelectronic shows a very interesting perspective as it can serve as a link between electronics and photonics. This will lead to Integrated Optics and hybrid ICs. Nanosensors are being realized using carbon nanotubes, this can easily lead to smart IC including MEMS and NEMS.

5. Conclusion

Despite the spectacular properties of SWCNTs, researchers must overcome many serious obstacles before a SWCNT-based nanoelectronic and nanotechnology can be implemented. The main difficulty involves the synthesis of a homogeneous SWCNT material. Currently used techniques produce a mixture of different-diameter semiconducting and metallic SWCNTs. Recently, however, significant progress has been made toward a more selective synthesis. The high density integration problem will slow down the development of the new data processors based on CNFETs. Lot of perseverance and efforts should be done towards this problem. However, this will help in removal of the Si-Nanoelectronics limitations related to
capacitive effects in high frequency operations. Interconnects may be achieved using metallic CN that can conduct information using light beams.

References